IN THE SPECIFICATION

Please amend the paragraph within the specification beginning on page 6, line 18 with the following:

The upsampled digital audio signal is supplied to the input of the variable hold circuit 55, which supplies output samples at a rate $2^q.F_s'$, in response to the control signal applied to the control signal input 70. In response to the control signal, it is decided whether the next output sample ~~os~~ is obtained by taking over a new input sample or by repeating the previous output sample.

Please amend the paragraph within the specification beginning on page 6, line 32 with the following:

If the clock frequency of the sigma delta modulator 67 is F_x, it will generate F_x pulses in one second. Suppose now that this clock frequency is chosen to be the same as the output sampling frequency of the sampling rate converter, then the output pulses of the sigma delta modulator 67 can be used to control the conversion process. The input signal of the sigma delta modulator 67 is a DC value which is dependent of the input and output sampling frequencies of the sampling rate converter. The variable hold circuit 55 is controlled in such a way by means of the pulses supplied by the sigma delta modulator 67 that a '+1' pulse means that the previous output sample ~~isa~~ is repeated and that a '-1' pulse means that a new input sample is taken over.